UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/538,670	03/30/2000	Alan David Berenbaum	Berenbaum 7-2-3-3	8309

7590 03/25/2004

Kevin M Mason
Ryan & Mason L L P
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
DONAGHUE, LARRY D	

ART UNIT	PAPER NUMBER
2154	11

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 11

Application Number: 09/538,670
Filing Date: March 30, 2000
Appellant(s): BERENBAUM ET AL.

Kevin M. Mason
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/11/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-16 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,404,469	Chung et al.	4-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (5,404,469).

3. Chung et al. taught a multithreaded VLIW (col. 5, lines 40-62) including a plurality of functional units (110) executing instructions from instruction stream threads having a priority (col. 3, lines 54-65) and an allocator for selecting and forwarding the instructions to the functional units based on the priority (col. 3, line 54 - col. 4, line 63, col. 3, lines 8-29, col. 7, lines 20-40, col. 8, lines 32-55) and wherein the functional units can be allocated independently to any thread in the multithreaded instruction stream (col. 4, lines 11-63).

As to claim 2, Chung et al. taught the thread priority allows different threads to have different priorities (col. 3, lines 54-65).

As to claim 3, the allocator selects from the thread with the highest priority (col. 3, line 54- col. 4, line 63).

As to claim 4, Chung et al. taught allocator selects instructions as based on priority (col. 3, line 54- col. 4, line 63) and the availability of resources (col. 3, lines 8-29).

Claims 5, 9, 12, 15 and 16 fail to teach or define claims 1-4 and are rejected for the reasons set forth, above.

As to claims 6 and 13, Chung et al. taught allocating the instruction if the resources is available in the next cycle (col. 3, line 54 - col. 4, line 64).

As to claims 7 and 14, Chung et al. taught the resource is a functional unit (110).

As to claim 8, Chung et al. taught allocator selects instructions as based on priority (col. 3, line 54- col. 4, line 63) and the availability of resources (col. 3, lines 8-29).

As to claim 10, Chung et al. taught the thread priority allows different threads to have different priorities (col. 3, lines 54-65).

As to claim 11, the allocator selects from the thread with the highest priority (col. 3, line 54- col. 4, line 63).

(11) Response to Argument

The Examiner asserts that Chung teaches an allocator for selecting and forwarding the instructions to the functional units based on the priority (col. 3, line 54, to col. 4, line 63; col. 3, lines 8-29; col. 7, lines 20-40; col. 8, lines 32-55).

Applicants note that, although Chung teaches that instructions are allocated to functional units, the allocation of instructions is not done independently of the type of instruction ready for execution within each thread. Chung teaches that "the processor 100 comprises four function units FU1, FU2, FU3, FU4. Illustratively, FU1 is an arithmetic unit, FU2 is a logic unit, FU3 is a load/store unit and FU4 is a branch unit." Col. 7, lines 43-46. Thus, each functional unit is dedicated to executing particular types of instructions and, therefore, each functional unit can only be allocated to a thread that has an instruction ready for execution wherein the instruction type matches the capability of the functional unit. The allocation of the functional units is dependent on the type of instructions ready for execution within each thread. Independent claims 1, 5, 9, 12, 15, and 16 require <u>independently allocating said functional units to any thread in said multithreaded instruction stream</u>. This feature is supported in the specification on page 6, lines 21-23, (of the substitute specification) wherein it is disclosed that "the illustrative Multithreaded VLIW processor 600 includes nine functional units 620-1 through 620-9, which can be allocated independently to any thread TA-TC." (emphasis added)

RESPONSE

Applicant asserts that the allocation of instructions as taught by Chung is not done independently of the type of instruction ready for execution within each thread.

This is not claimed or disclosed in the instant application.

What is set forth on page 6, lines 21-23 is that the functional units are independently allocated to the threads, (instructions from multiple threads can be allocate in a single cycle, fig. 6) not that the allocation is independent of the instruction type.

Further note claim 5, "said allocator selecting instructions based on resource availability and independently allocating said functional units to any thread in said multithreaded instruction stream". (emphasis added)

Claim 6, " ... resource availability allows said instructions to be allocated only if the resource required by the instruction are available for the next cycle."

Claim 7, set forth "resources comprise functional units."

This clearly set forth in the claims that the instructions are allocated based on the availability of functional unit and that instructions allocated only if the required functional unit is available.

Page 7, line 9-10, " ... a decode stage 720, where the required functional units and registers are identified for the fetched instructions, ..."

Identifying the required functional unit is conventional done of the basis of type of instruction , load/store instructions go to the load/store/unit , integer instructions to the integer unit , etc.

As show by claims 5 –7 and the specification of the instant application the allocating of functional unit is not done independent of the instruction type.

For the above reasons, it is believed that the rejections should be sustained.

Andrew Caldwell
Andrew Caldwell

Respectfully submitted,

March 20, 2004

Conferees

ZARNI MAUNG
PRIMARY EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

Kevin M Mason
Ryan & Mason L L P
90 Forest Avenue
Locust Valley, NY 11560